CLAIM AMENDMENTS

Claim 1 (canceled)

2. **(new)** A microcontroller comprising:

a central processing unit;

a data memory having a linearized address space coupled with said central processing unit being divided into *n* banks;

said central processing unit comprising:

a bank select unit which either accesses one of said banks or accesses a virtual bank, whereby said virtual bank combines partial memory space of two banks of said data memory and wherein said selected bank forms a register file;

an arithmetic logic unit coupled with said register file;

a plurality of special function registers being mapped to one of said banks in said data memory, wherein one of said special function registers is a working register being coupled with said arithmetic logic unit;

a program counter register within said central processing unit, said program counter mapped in said data memory; and

a working register within said central processing unit being coupled with said arithmetic logic unit, said working register mapped in said data memory;

wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit indicating whether said bank select unit accesses one of said banks or said virtual bank.

3. **(new)** A microcontroller as in claim 2 wherein said instruction set includes an instruction with an encoding of 1110 110s kkkk kkkk 1111 kkkk kkkk kkkk, wherein said instruction is a subroutine call of an entire 2 mega byte memory range, said 's' bit of said instruction is used to modify the behavior of said instruction, said memory range designated by said kkkk kkkk and kkkk kkkk kkkk portions of said instruction.

4. **(new)** A microcontroller as in claim 2 wherein said instruction set includes an instruction with an encoding of 1110 1111 kkkk kkkk 1111 kkkk kkkk kkkk, wherein wherein said instruction provides an unconditional branch for a program composed from said instruction set anywhere within a 2 megabyte memory range designated by said kkkk kkkk and kkkk kkkk kkkk portions of said instruction.

5. **(new)** A microcontroller as in claim 2 wherein said instruction set includes an instruction with an encoding of 1111 xxxx xxxx xxxx, wherein said instruction performs no operation, and the contents of said xxxx xxxx xxxx portion of said instruction are ignored.

6. **(new)** A microcontroller as in claim 2 wherein said instruction set includes an instruction with an encoding of 0000 0000 0000 0000, wherein said instruction performs no operation, and the contents of the latter 0000 0000 0000 portion of said instruction are ignored.

7. **(new)** A microcontroller comprising:

a central processing unit;

a data memory coupled with said central processing unit being divided into *n* banks;

said central processing unit comprising:

a bank select unit for selecting one of said banks in said data memory, wherein said selected bank forms a register file;

an arithmetic logic unit coupled with said register file; and

a plurality of special function registers being mapped to one of said banks in said data memory;

wherein one of said special function registers is a working register being coupled with said arithmetic logic unit.

8. **(new)** A microcontroller as in claim 7 wherein said instruction set includes an instruction with an encoding of 1110 110s kkkk kkkk 1111 kkkk kkkk kkkk, wherein said instruction is a subroutine call of an entire 2 mega byte memory range, said 's' bit of said instruction is used to modify the behavior of said instruction, said memory range designated by said kkkk kkkk and kkkk kkkk kkkk portions of said instruction.

9. **(new)** A microcontroller as in claim 7 wherein said instruction set includes an instruction with an encoding of 1110 1111 kkkk kkkk 1111 kkkk kkkk kkkk, wherein said instruction provides an unconditional branch for a program composed from said instruction set anywhere within a 2 megabyte memory range designated by said kkkk kkkk and kkkk kkkk kkkk portions of said instruction.

10. **(new)** A microcontroller as in claim 7 wherein said instruction set includes an instruction with an encoding of 1111 xxxx xxxx xxxx, wherein said instruction performs no operation, and the contents of said xxxx xxxx xxxx portion of said instruction are ignored.

11. **(new)** A microcontroller as in claim 7 wherein said instruction set includes an instruction with an encoding of 0000 0000 0000 0000, wherein said instruction performs no operation, and the contents of the latter 0000 0000 0000 portion of said instruction are ignored.